WHAT IS CLAIMED IS:

1. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at preparation period; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output

terminal of the inverter at transmission period.

2. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the receiving capacitor to a predetermined voltage at preparation period; and

a latch for supplying an output digital signal obtained

by performing logic amplification of a voltage of the output terminal of the inverter at transmission period.

3. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at preparation period; and

a latch for holding an output digital signal obtained during a preceding transmission period at preparation period.

4. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch for setting a voltage in accordance with a logic level of a supplied input digital signal in the transmitting capacitor at preparation period; and

a transmitting switch for generating a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch for short-circuiting the input terminal and the output terminal of the inverter so as to set a voltage of the signal line to a predetermined voltage at preparation period; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

5. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a supplied input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at preparation period, and to be off for each transmission period; and

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

6. The signal transmission circuit according to claim 5, further comprising a cut-off switch for separating the inverter from a power line after the setting of the equalized voltage is completed at preparation period.

7. The signal transmission circuit according to claim 5, further comprising a cut-off switch for separating the inverter from a power line after a voltage of the output terminal of the inverter is established at transmission

period.

8. A signal transmission circuit for transmitting a digital signal from either one of a first circuit block group to a second circuit block via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

each of the first circuit block group comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a supplied input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at preparation period, and to be off for each transmission period;

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period; and

a logic circuit for changing each state of the input switch and the transmitting switch in response to the clock signal when a corresponding selection signal is activated, and for fixing each state of the input switch and the

transmitting switch when the selection signal is non-activated,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor; and

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

9. A signal transmission circuit for transmitting a digital signal from a first circuit block to either one of a second circuit block group via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a supplied input digital signal to the transmitting capacitor for each preparation period so as to set a voltage in accordance with a logic level of the input digital signal in the transmitting capacitor at preparation period, and to be off for each transmission period; and

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period;

each of the second circuit block group comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of

the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and discharge the receiving capacitor;

a latch for supplying an output digital signal obtained by performing logic amplification of a voltage of the output terminal of the inverter for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period; and

a logic circuit for changing a state of the equalizing switch in response to the clock signal when a corresponding selection signal is activated, and for fixing the equalizing switch to be off when the selection signal is non-activated.

10. A signal transmission circuit for transmitting a logic operation result from a first circuit block group to a second circuit block via a common signal line in synchronization with a clock signal that repeats a first logic level indicating a preparation period and a second logic level indicating a transmission period, the logic operation result being based on a digital signal supplied to each of the first circuit block group,

each of the first circuit block group comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a predetermined logic voltage to the transmitting capacitor for each preparation period so as to set the logic voltage in the transmitting capacitor at preparation period, and to be off

for each transmission period;

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period; and

a logic circuit for changing each state of the input switch and the transmitting switch in response to the clock signal when a corresponding input digital signal is activated, and for fixing each state of the input switch and the transmitting switch when the input digital signal is non-activated,

the second circuit block comprising a receiving circuit including:

an inverter connected to the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch designed to be on to short-circuit the input terminal and the output terminal of the inverter for each preparation period so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage at preparation period, and to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line for each transmission period so as to charge and

discharge the receiving capacitor; and

a latch for amplifying a voltage of the output terminal of the inverter by performing logical determination with a logic threshold voltage different from the equalized voltage so that an output digital signal indicating the logic operation result is obtained for each transmission period and holding the output digital signal obtained during a preceding transmission period for each preparation period.

11. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line,

the first circuit block comprising a transmitting circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

a precharge switch for setting a predetermined logic high voltage in the first transmitting capacitor at each low level period;

a first transmitting switch for generating a small voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding

low level period;

a predischarge switch for setting a predetermined logic low voltage in the second transmitting capacitor at each high level period; and

a second transmitting switch for generating a small voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

the second circuit block comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

an output circuit for supplying an output digital signal having a logic level in accordance with a logic level

of the input digital signal, in accordance with the first and second detection signals; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set a voltage of the receiving capacitor to a predetermined voltage.

12. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line,

the first circuit block comprising a transmitting circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a low level period during which a logic high level is output to the signal line, and a high level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

a precharge switch for setting a predetermined logic high voltage in the first transmitting capacitor at each low level period;

a first transmitting switch for generating a small voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

a predischarge switch for setting a predetermined logic low voltage in the second transmitting capacitor at each high level period; and

a second transmitting switch for generating a small voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

the second circuit block comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

an output circuit for supplying an output digital signal having a logic level in accordance with a logic level of the input digital signal, in accordance with the first and

second detection signals; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set a voltage of the receiving capacitor to a predetermined voltage.

13. A signal transmission circuit for transmitting a digital signal from a first circuit block to a second circuit block via a signal line,

the first circuit block comprising a transmitting circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

a precharge switch designed to be on to supply a predetermined logic high voltage to the first transmitting capacitor for each low level period so as to set the logic high voltage to the first transmitting capacitor at each low level period, and to be off for each high level period;

a first transmitting switch designed to be on to connect the first transmitting capacitor to the signal line for a certain period from a start time of each high level period so as to generate a small positive voltage change in

the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

a predischarge switch designed to be on to supply a predetermined logic low voltage to the second transmitting capacitor for each high level period so as to set the logic low voltage in the second transmitting capacitor at each high level period, and to be off for each low level period; and

a second transmitting switch designed to be on to connect the second transmitting capacitor to the signal line for a certain period from a start time of each low level period so as to generate a small negative voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

the second circuit block comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a latch that is set and reset in accordance with the first and second detection signals so as to supply an output digital signal having a logic level in accordance with a logic level of the input digital signal; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

14. The signal transmission circuit according to claim 13, wherein the first level circuit is constituted by an inverter having a logic threshold voltage lower than the equalized voltage, and the second level circuit is constituted by an inverter having a logic threshold voltage higher than the equalized voltage.

15. The signal transmission circuit according to claim 13, wherein the receiving circuit further comprises an input terminal of a reset signal for forcing the equalizing switch

to be on.

16. A transmitting circuit for transmitting a digital signal to a signal line, comprising:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input digital signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

a precharge switch designed to be on to supply a predetermined logic high voltage to the first transmitting capacitor for each low level period so as to set the logic high voltage to the first transmitting capacitor at each low level period, and to be off for each high level period;

a first transmitting switch designed to be on to connect the first transmitting capacitor to the signal line for a certain period from a start time of each high level period so as to generate a small positive voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

a predischarge switch designed to be on to supply a predetermined logic low voltage to the second transmitting capacitor for each high level period so as to set the logic low voltage in the second transmitting capacitor at each high level period, and to be off for each low level period; and

a second transmitting switch designed to be on to connect the second transmitting capacitor to the signal line for a certain period from a start time of each low level period so as to generate a small negative voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period.

17. A receiving circuit for receiving a digital signal from a signal line, comprising:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a latch that is set and reset in accordance with the first and second detection signals so as to supply an output digital signal having a logic level in accordance with a logic level of the input digital signal; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

18. A signal transmission circuit for transmitting a clock signal from a first circuit block to each of a second circuit block group via a common signal line,

the first circuit block comprising a transmitting circuit including:

a transition detection circuit for sequentially detecting a transition of a logic level of a supplied input clock signal so as to detect a high level period during which a logic high level is output to the signal line, and a low level period during which a logic low level is output to the signal line;

first and second transmitting capacitors;

a precharge switch designed to be on to supply a predetermined logic high voltage to the first transmitting capacitor for each low level period so as to set the logic high voltage to the first transmitting capacitor at each low level period, and to be off for each high level period;

a first transmitting switch designed to be on to connect the first transmitting capacitor to the signal line for a certain period from a start time of each high level period so as to generate a small positive voltage change in the signal line at each high level period, the voltage change being in accordance with a voltage of the first transmitting capacitor that is set during a preceding low level period;

a predischarge switch designed to be on to supply a predetermined logic low voltage to the second transmitting capacitor for each high level period so as to set the logic low voltage in the second transmitting capacitor at each high level period, and to be off for each low level period; and

a second transmitting switch designed to be on to connect the second transmitting capacitor to the signal line for a certain period from a start time of each low level period so as to generate a small negative voltage change in the signal line at each low level period, the voltage change being in accordance with a voltage of the second transmitting capacitor that is set during a preceding high level period,

each of the second circuit block group comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a first level circuit for supplying a first detection signal when a small positive voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a second level circuit for supplying a second detection signal when a small negative voltage change in the signal line is detected from a voltage of the output terminal of the inverter;

a latch that is set and reset in accordance with the first and second detection signals so as to supply an output clock signal having a logic level in accordance with a logic level of the input clock signal; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the first detection signal or the second detection signal is supplied so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.

19. A signal transmission circuit for transmitting a clock signal from a first circuit block to each of a second circuit block group via a common signal line,

the first circuit block comprising a transmitting circuit including:

a transmitting capacitor;

an input switch designed to be on to supply a predetermined logic voltage to the transmitting capacitor for each preparation period so as to set the logic voltage in the transmitting capacitor at preparation period during which an supplied input clock signal is at a first logic level, and to be off for each transmission period during which the input clock signal is at a second logic level; and

a transmitting switch designed to be on to connect the transmitting capacitor to the signal line for each transmission period so as to generate a small voltage change in the signal line at transmission period, the voltage change being in accordance with a voltage of the transmitting capacitor that is set during a preceding preparation period, and to be off for each preparation period,

each of the second circuit block group comprising a receiving circuit including:

an inverter for amplifying a small voltage change in the signal line;

a receiving capacitor inserted between an input terminal and an output terminal of the inverter;

an equalizing switch inserted between the input terminal and the output terminal of the inverter;

a level circuit for supplying a pulse of an output clock signal when a small voltage change in the signal line is detected from a voltage of the output terminal of the inverter; and

an equalizing control circuit for forcing the equalizing switch to be on for a certain period after the small voltage change in the signal line is detected so as to set each voltage of the signal line and the input terminal and the output terminal of the inverter to a predetermined equalized voltage, and forcing the equalizing switch to be off to allow an operation of the inverter for amplifying a small voltage change in the signal line to charge and discharge the receiving capacitor for other periods.